EE 435

Lecture 18

- Moving the RHP zero into LHP in Miller Compensated Amplifier
- Breaking the Loop for Loop Gain Analysis

Relationship between pole Q and phase margin

In general, the relationship between the phase margin and the pole Q is dependent upon the order of the transfer function and on the location of the zeros

In the special case that the open loop amplifier is second-order low-pass, a closed form analytical relationship between pole Q and phase margin exists and this is independent of A_0 and β..

$$Q = \frac{\sqrt{\cos(\varphi_M)}}{\sin(\varphi_M)} \qquad \varphi_M = \cos^{-1}\left(\sqrt{1+\frac{1}{4Q^4}} - \frac{1}{2Q^2}\right)$$

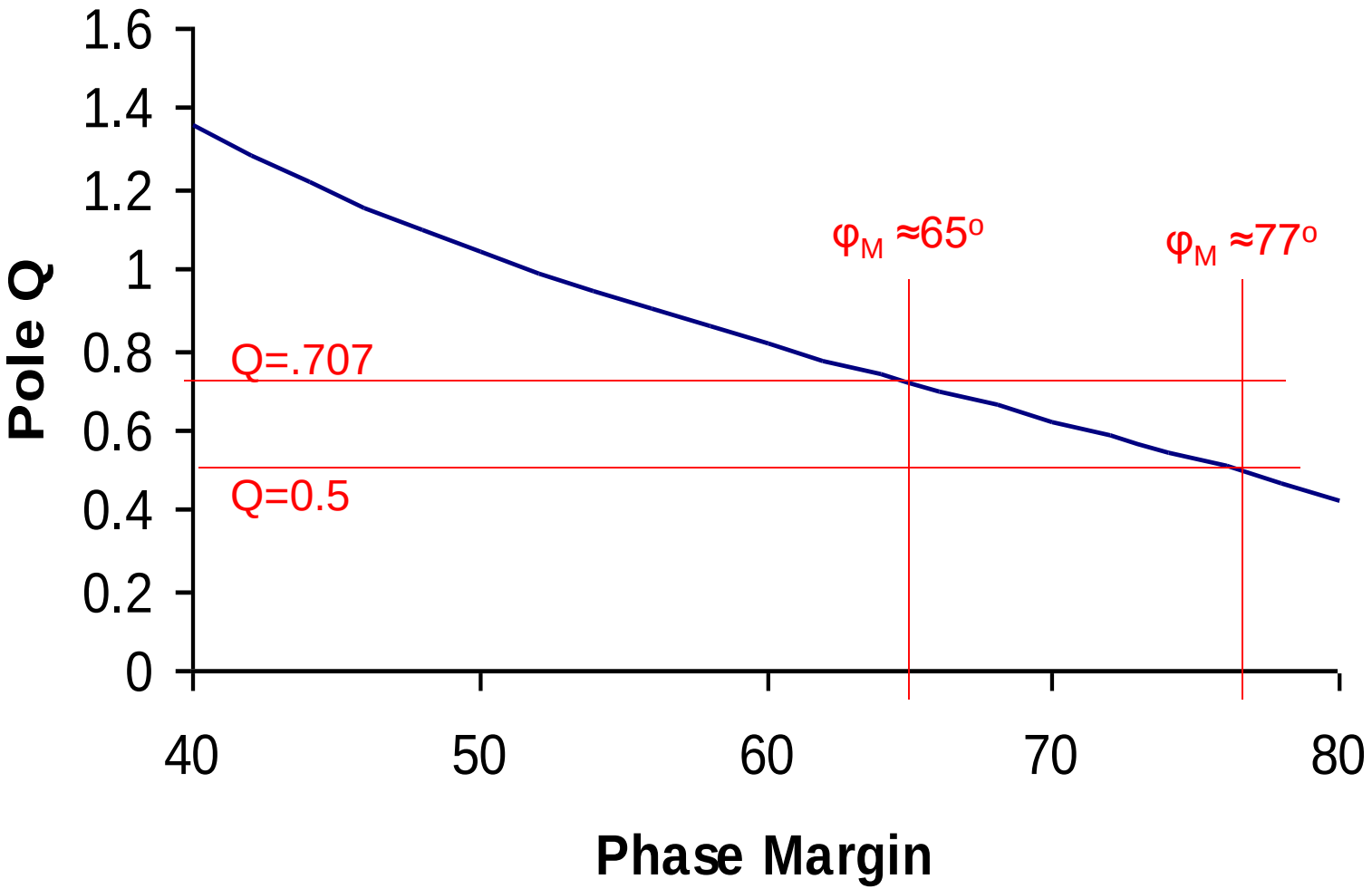
The region of interest is invariable only for $0.5 < Q < 0.7$

larger Q introduces unacceptable ringing and settling

smaller Q slows the amplifier down too much

Phase Margin vs Q

Second-order low-pass Amplifier



.707< Q <0.5 ⇒ **65° < φ_M < 75°**

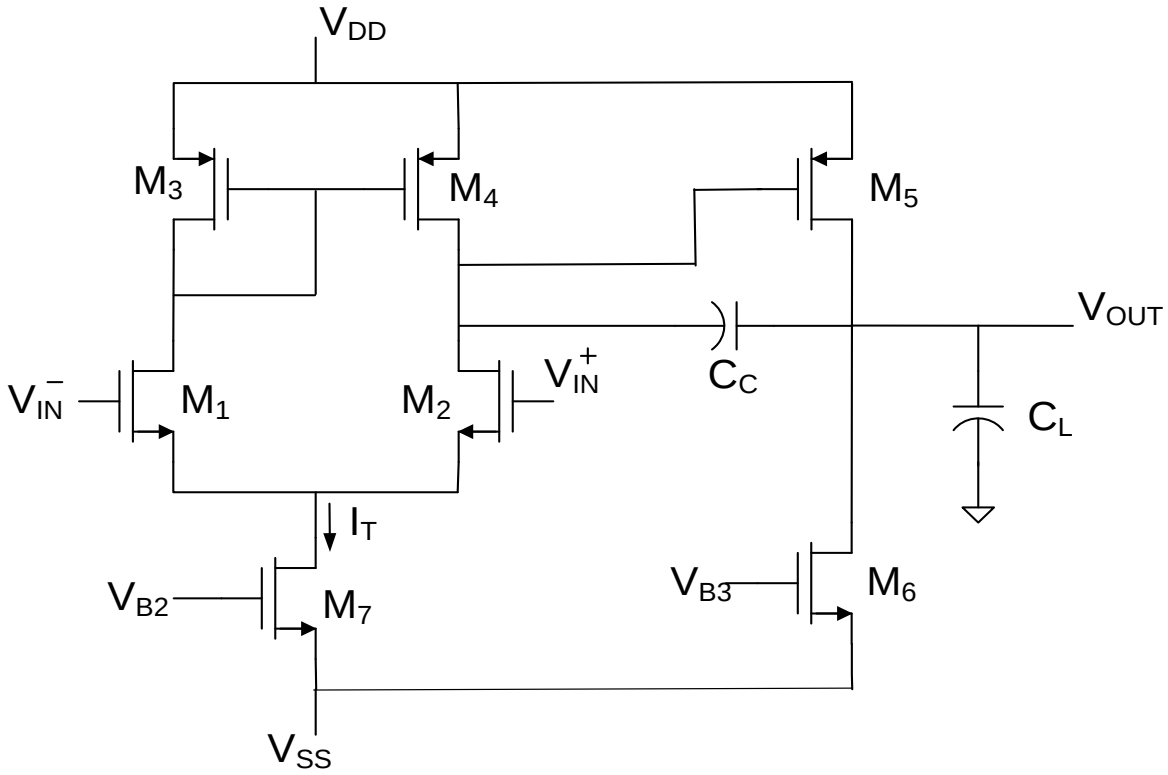
Compensation Summary

- Gain and phase margin performance often strongly dependent upon architecture
- Relationship between overshoot and ringing and phase margin were developed only for 2^{nd}-order lowpass gain characteristics and differ dramatically for higher-order structures
- Absolute gain and phase margin criteria are not robust to changes in architecture or order
- It is often difficult to correctly “break the loop” to determine the loop gain Aβ with the correct loading on the loop (will discuss this more later)

Design of Two-Stage Op Amps

- Compensation is critical in two-stage op amps
- General approach to designing two-stage op amps is common even though significant differences in performance for different architectures
- Will consider initially the most basic two-stage op amp with internal Miller compensation

Natural Parameter Space for the Two-Stage Amplifier Design



$$S_{NATURAL} = \{W_1, L_1, W_3, L_3, W_5, L_5, W_6, L_6, W_7, L_7, I_T, I_{D6}, C_c\}$$

Parameter Inter-dependence

I_T affects

$$A_O \cong \frac{g_{md} g_{mo}}{g_{oo} g_{od}}$$

$$GB \cong \frac{g_{md}}{C_C}$$

$$SR \cong \frac{I_T}{C_C}$$

$$g_{md} \cong \frac{1}{2}\sqrt{\mu C_{OX} \frac{W_1}{L_1}}\sqrt{I_T}$$

Review from last lecture

Practical Set of Design Parameters

$$S_{PRACTICAL} = \{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}$$

7 degrees of freedom!

- P : total power dissipation
- θ = fraction of total power in second stage
- V_{EBk} = excess bias voltage for the k^{th} transistor
- Phase margin constraint assumed (so C_C not shown in DoF)

Example for Design Procedure

Summary of Design Procedure for This Set of Specifications and this Architecture:

1. Choose channel length
2. Select: V_{EB3}, V_{EB5}, V_{EB6}
3. Select: V_{EB1}
4. Select: V_{EB7}
5. Choose P to satisfy power constraint
6. Choose θ to meet GB constraint
7. Compensation capacitance C_C
8. Calculate all transistor sizes
9. Implement structure, simulate, and make modifications if necessary guided by where deviations may occur

Note: Though not shown, this design procedure was based upon looking at the set of equations that must be solved and developing a sequence to solve these equations. It may not always be the case that equations can be solved sequentially.

Note: Different specification requirements (constraints) will generally require a different design procedure

Power distribution between stages

Note: Optimum power split for previous example was for dominant pole compensation in first stage. Results may be different for Miller compensation or for output compensation

For first-stage compensation capacitor with compensation criteria $p_2=3\beta A_0 p_1$:

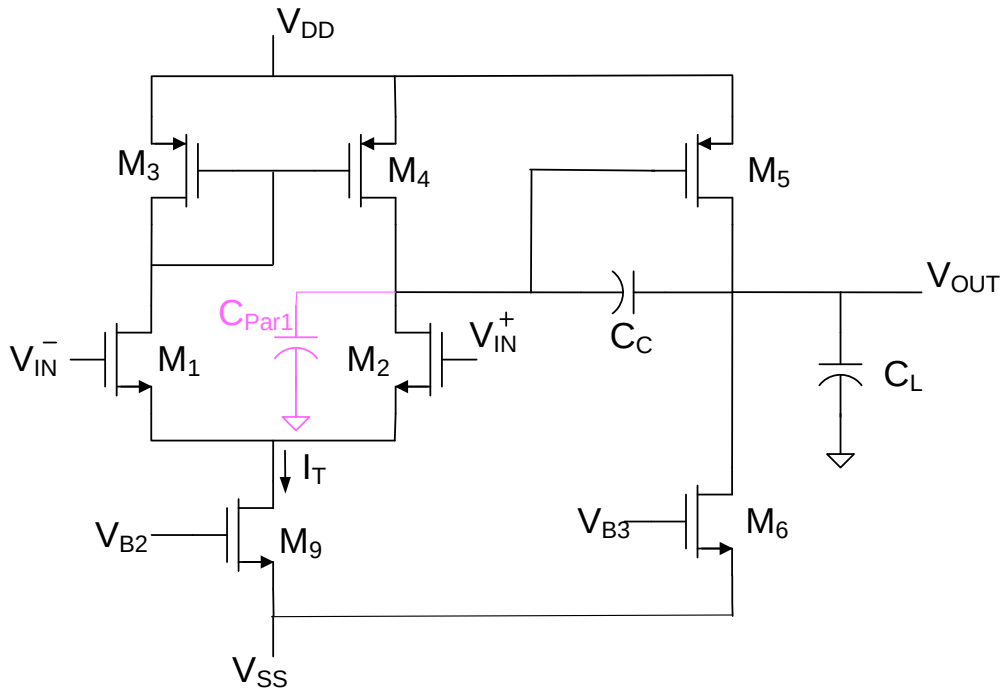
$$GB = \frac{\left(\lambda_p + \lambda_n\right)\theta P}{V_{DD} 3\beta C_L}$$

For Miller Compensation with RHP zero and arbitrary Q compensation criteria:

$$GB = \frac{P(1-\theta)}{V_{DD} V_{EB1} C_C} = \frac{PQ^2\left(2\theta V_{EB1} - \beta(1-\theta)\left|V_{EB5}\right|\right)^2}{C_L \beta 2\theta V_{EB1}^2 \left|V_{EB5}\right| V_{DD}}$$

By taking derivative of GB wrt θ, it can be easily shown that the derivative is positive in the interval $0<\theta\leq 1$ indicating that for a given P, want to make θ close to 1 to maximize GB

Basic Two-Stage Op Amp

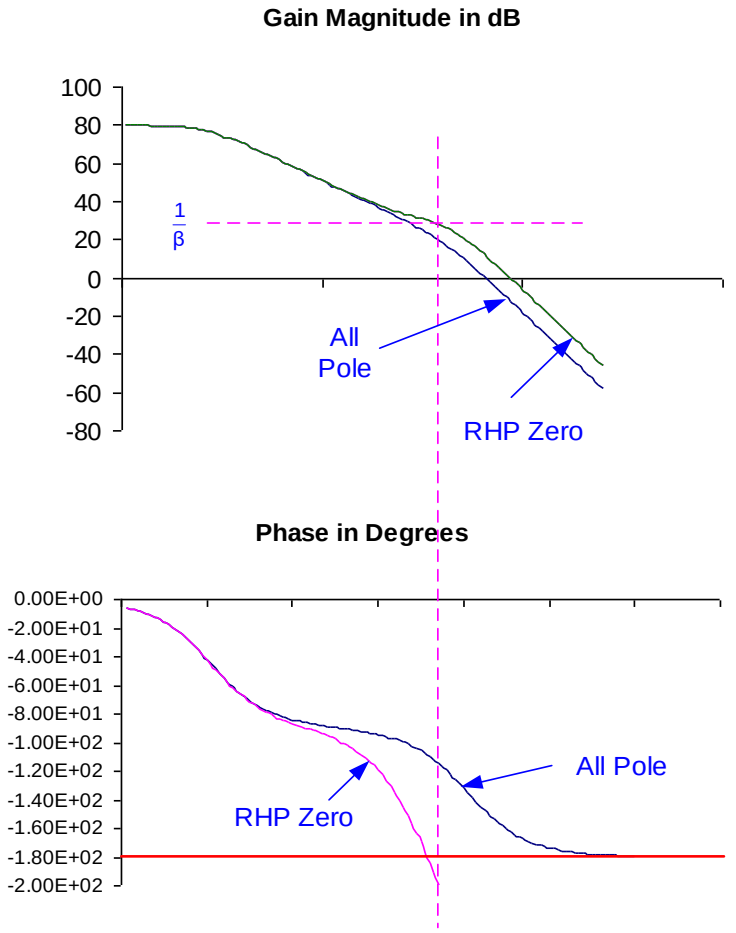


$$A_{FB}(s) \cong \frac{g_{md}\left(g_{m0} - sC_c\right)}{s^2 C_C C_L + sC_C\left(g_{mo} - \beta\, g_{md}\right) + \beta\, g_{md} g_{mo}}$$

Right Half-Plane Zero Limits Performance

- Why does the RHP zero limit performance ?
- Can anything be done about this problem ?
- Why is this not 3rd order since there are 3 caps ?

Why does the RHP zero limit performance ?

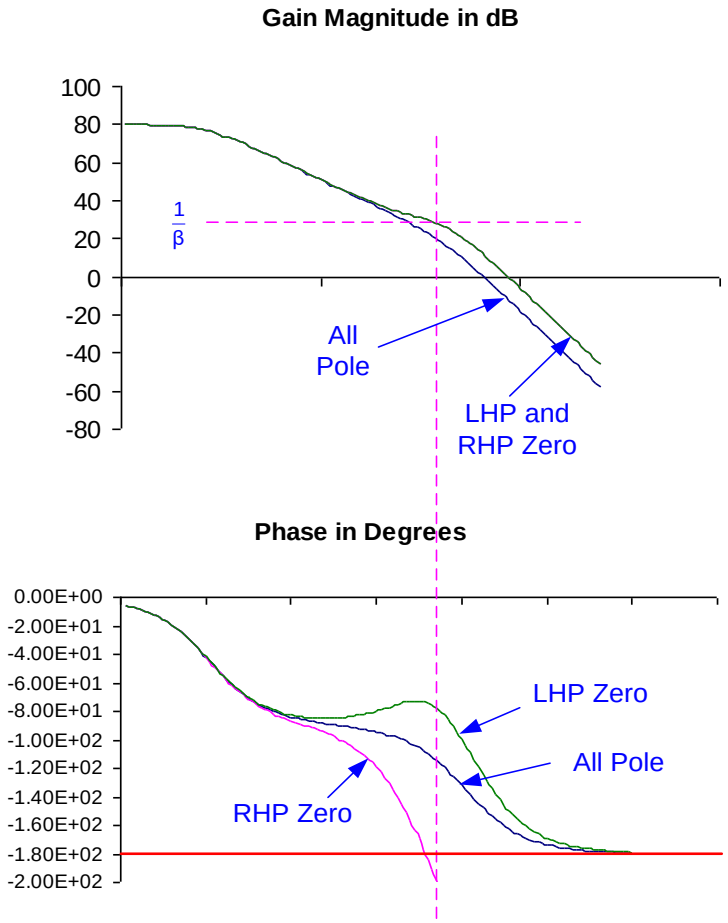


p_1= -1, p_2= -1000, z_x={none, +250}

In this example:

- accumulate phase shift and slow gain drop with RHP zeros
- effects are dramatic

Why does the RHP zero limit performance ?



p_1=1, p_2=1000, z_x={none,250,-250}

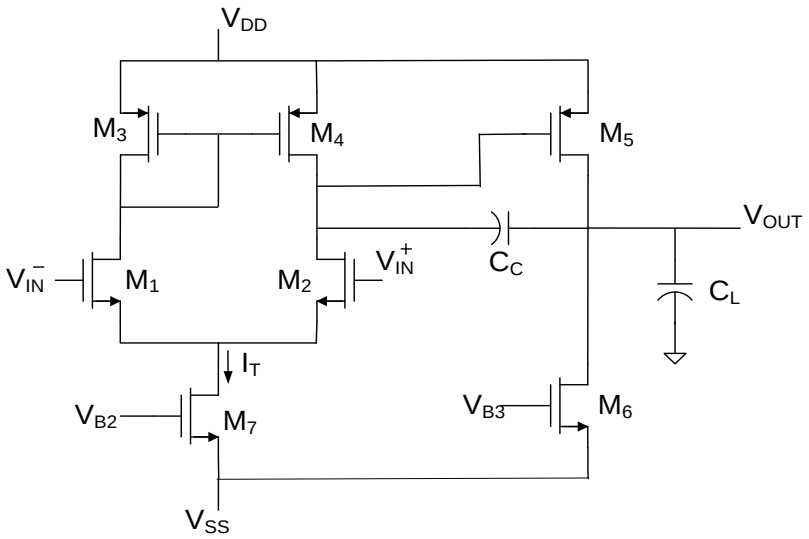
In this example:

- accumulate phase shift and slow gain drop with RHP zeros
- loose phase shift and slow gain drop with LHP zeros
- effects are dramatic

Two-stage amplifier

(with RHP Zero Compensation)

What causes the Miller compensation capacitor to create a RHP zero?



$$V_d = V_{IN}^{+} - V_{IN}^{-}$$

$$A_V = (A_0 p_1 p_2)\frac{1}{(s+p_1)(s+p_2)}$$

with Miller Compensation

$$A_V = \left(A_0 \frac{p_1 p_2}{z}\right)\frac{-s+z}{(s+p_1)(s+p_2)}$$

At low frequencies, V_{OUT}/V_d is positive but at high frequencies it becomes negative

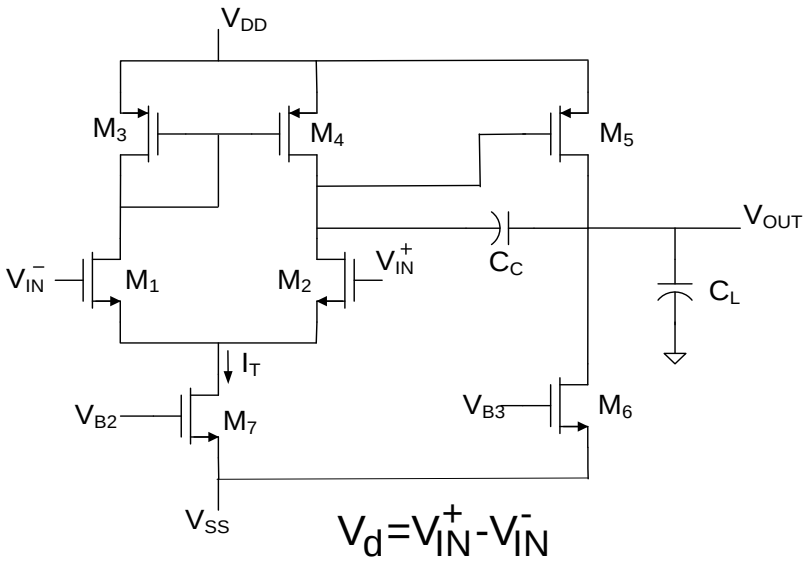
Alternately, C_C provides a feed-forward inverting signal from the input to the first stage output which also becomes the second stage output

Feed-forward paths create zeros in the gain transfer function !

Two-stage amplifier

(with RHP Zero Compensation)

What can be done to remove the RHP zero?



$$A_V = (A_0 p_1 p_2)\frac{1}{(s+p_1)(s+p_2)}$$

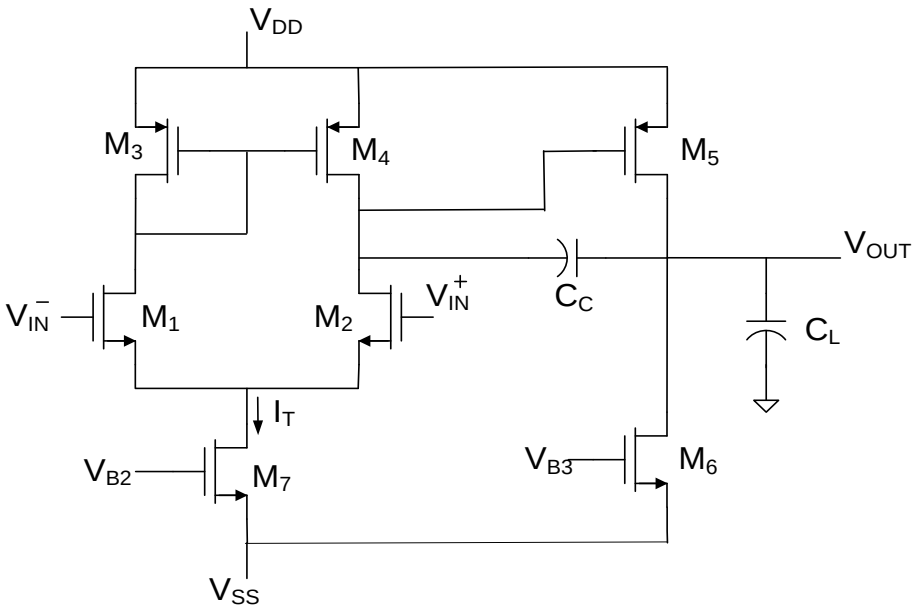
with Miller Compensation

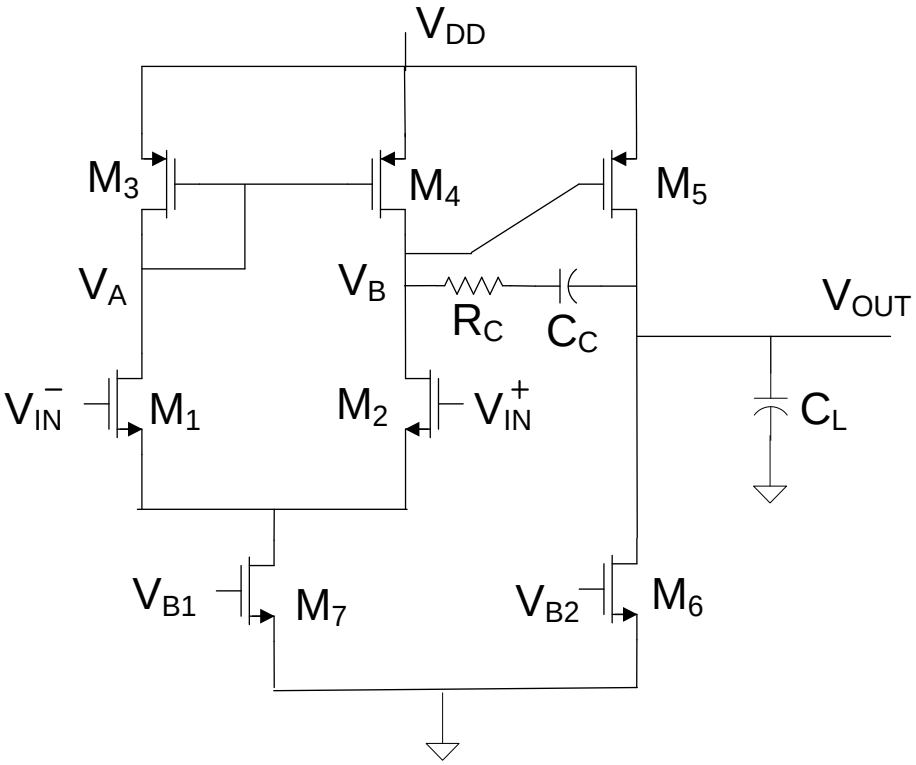
$$A_V = \left(A_0 \frac{p_1 p_2}{z}\right)\frac{-s+z}{(s+p_1)(s+p_2)}$$

Alternately, C_C provides a feed-forward inverting signal from the input to the first stage output which also becomes the second stage output

Break the feed-forward path from the output of the first stage to the output of the second stage at high frequencies

Two-stage amplifier with LHP Zero Compensation





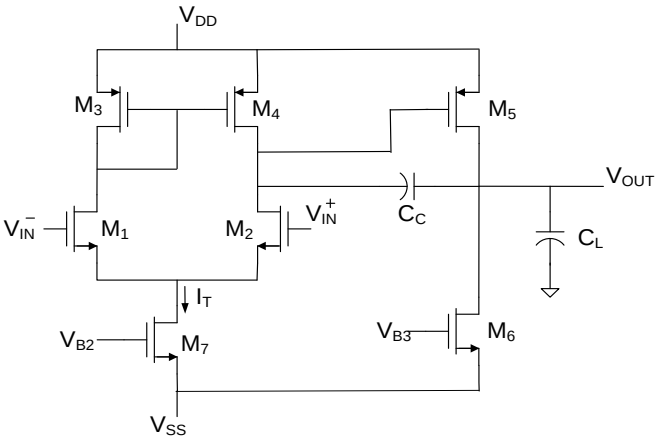
Right Half-Plane Zero Limits Performance

Will show zero can be moved to Left Half-Plane

R_C realized with single triode region device

Two-stage amplifier with LHP Zero Compensation

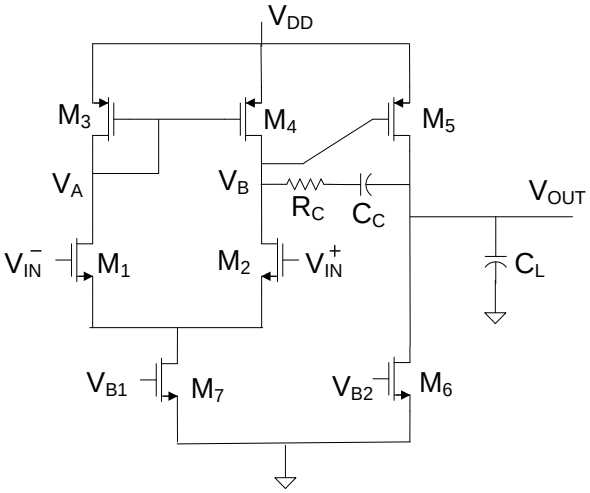
Analysis almost by inspection:



$$A(s) = \frac{g_{md}\left(g_{m5} - sC_c\right)}{s^2 C_C C_L + sC_C g_{m5} + g_{oo} g_{od}}$$

$$\frac{1}{sC_c} \quad \Rightarrow \quad \frac{1}{sC_c} + R_C$$

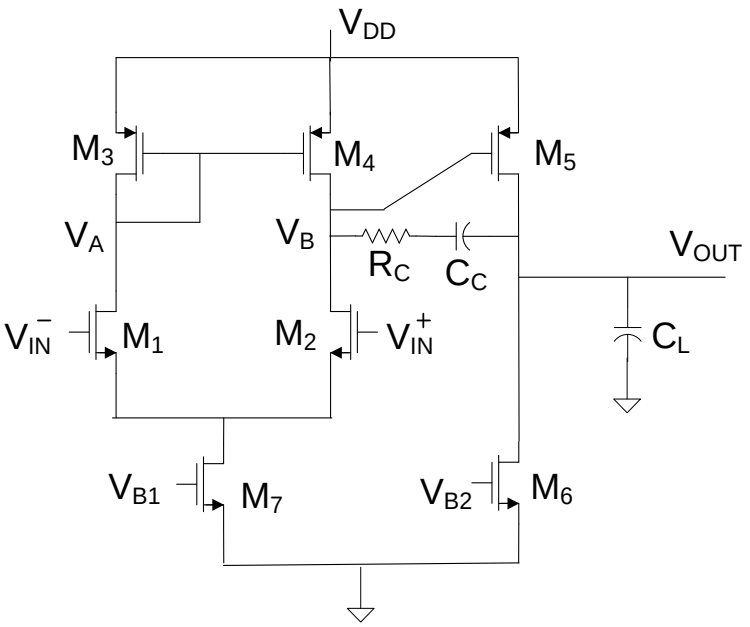
$$sC_C \quad \Rightarrow \quad \frac{sC_c}{1 + sC_c R_C}$$



$$A(s) = \frac{g_{md}\left(g_{m5} + sC_c\left[\frac{g_{m5}}{g_c} - 1\right]\right)}{s^2 C_C C_L + sC_C g_{m5} + g_{oo} g_{od}}$$

$$z_1 = \frac{-g_{m5}}{C_C\left[\frac{g_{m5}}{g_C} - 1\right]}$$

Two-stage amplifier with LHP Zero Compensation



$$A(s) = \frac{g_{md}\left(g_{m5} + sC_c\left[\frac{g_{m5}}{g_c} - 1\right]\right)}{s^2 C_C C_L + sC_C g_{m5} + g_{oo} g_{od}}$$

$$z_1 = \frac{-g_{m5}}{C_C\left[\frac{g_{m5}}{g_C} - 1\right]}$$

z_1 location can be programmed by R_C

If $g_c > g_{m5}$, z_1 in RHP and if $g_c < g_{m5}$, z_1 in LHP

R_C has almost no effect on p_1 and p_2

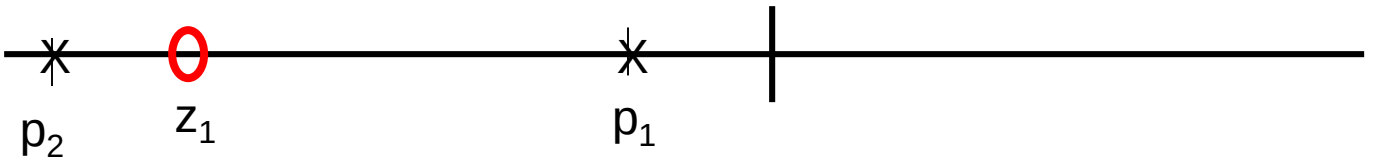
Two-stage amplifier with LHP Zero Compensation

$$A(s) = \frac{g_{md}\left(g_{m5} + sC_c\left[\frac{g_{m5}}{g_c} - 1\right]\right)}{s^2 C_C C_L + sC_C g_{m5} + g_{oo} g_{od}}$$

$$z_1 = \frac{-g_{m5}}{C_C\left[\frac{g_{m5}}{g_C} - 1\right]}$$

$$p_1 = -\frac{g_{o1} + g_{o5}}{C_C\left(\frac{g_{m5}}{g_{05} + g_{o6}}\right)}$$

$$p_2 = -\frac{g_{m5}}{C_L}$$

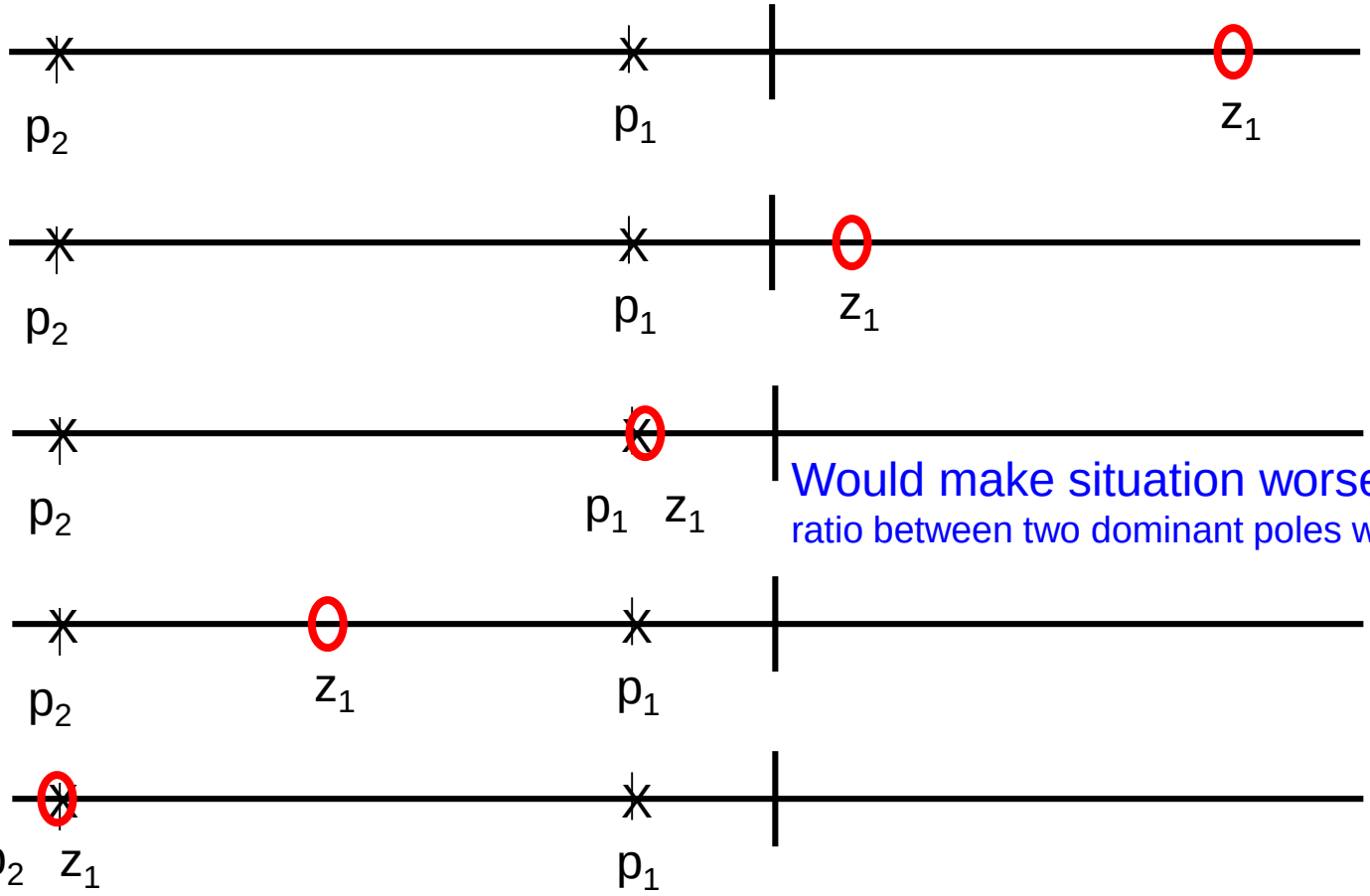


where should z_1 be placed?

Two-stage amplifier with LHP Zero Compensation

where should z_1 be placed?

$$z_1 = \frac{-g_{m5}}{C_C\left[\frac{g_{m5}}{g_C} - 1\right]}$$



$$p_1 = -\frac{g_{o1} + g_{o5}}{C_C\left(\frac{g_{m5}}{g_{o5} + g_{o6}}\right)}$$

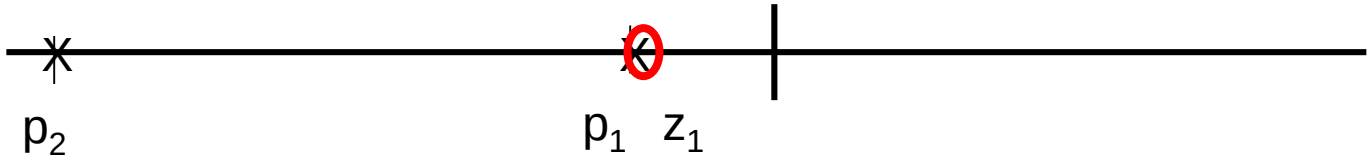
$$p_2 = -\frac{g_{m5}}{C_L}$$

Would make situation worse (because ratio between two dominant poles would be reduced !

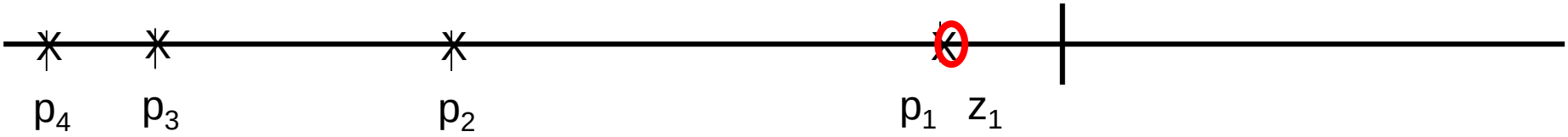
Two-stage amplifier with LHP Zero Compensation

where should z_1 be placed?

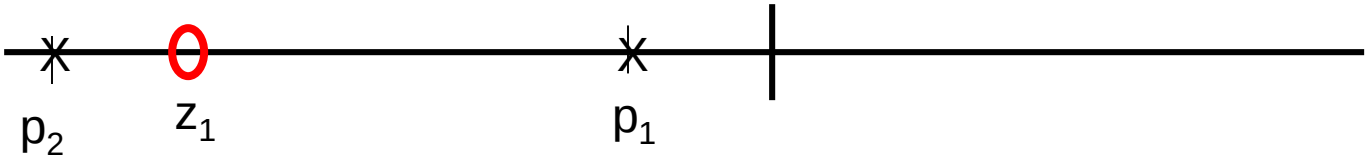
Would make situation worse (because ratio between two dominant poles would be reduced !



Other parasitic poles, at higher frequencies are present and not too much larger than p_2!



Two-stage amplifier with LHP Zero Compensation



$$z_1 = \frac{-g_{m5}}{C_C\left[\frac{g_{m5}}{g_C} - 1\right]}$$

z_1 often used to cancel p_2

Can reduce size of required compensation capacitor

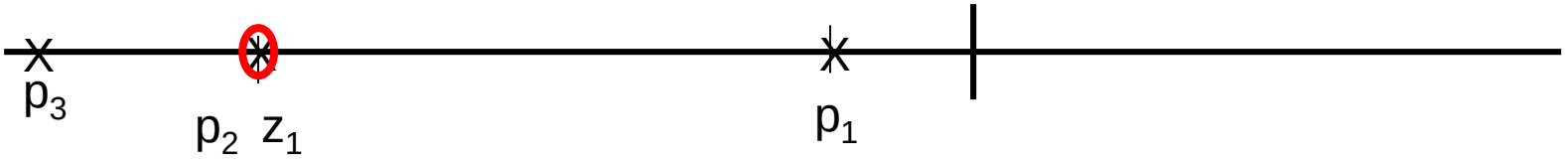
a) eliminates RHP zero

b) increases spread between p_1 and p_3

Improves phase margin

Design formulations easily extend to this structure

Two-stage amplifier with LHP Zero Compensation

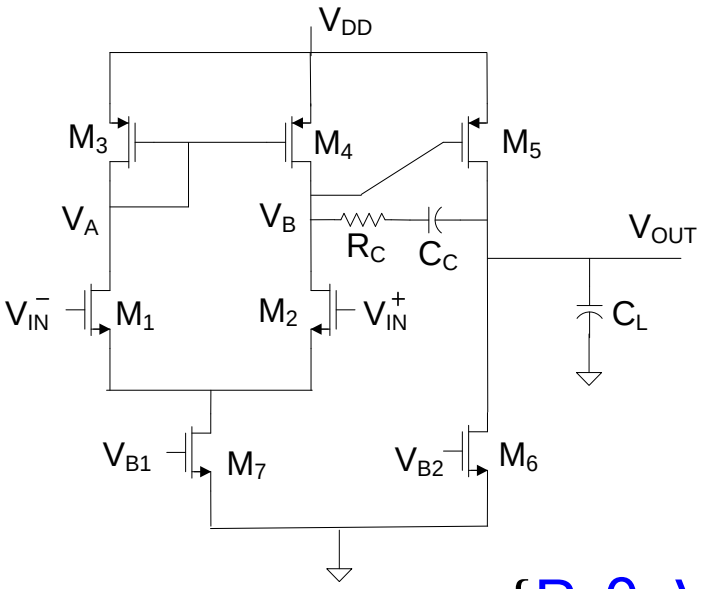


$$z_1 = \frac{-g_{m5}}{C_C\left[\frac{g_{m5}}{g_C} - 1\right]}$$

Analytical formulation for compensation requirements not easy to obtain
(must consider at least 3rd –order poles and both T(s) and poles not mathematically tractable)

C_C often chosen to meet phase margin (or settling/overshoot) requirements after all other degrees of freedom used with computer simulation from magnitude and phase plots

Basic Two-Stage Op Amp with LHP zero



8 Degrees of Freedom

$$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}, R_C, C_C\}$$

1 constraint (phase margin)

---

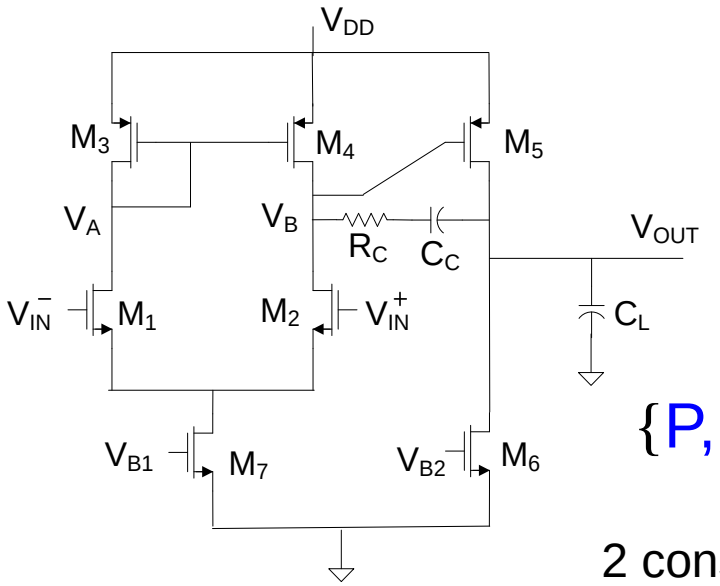
with zero cancellation of p_2

7 Degrees of Freedom

$$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}, R_C, C_C\}$$

2 constraints (phase margin), $z_1 = p_2 = \dfrac{-g_{m5}}{C_C\left[\dfrac{g_{m5}}{g_C} - 1\right]}$

Basic Two-Stage Op Amp with LHP zero



with zero cancellation of p_2

7 Degrees of Freedom

$$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}, R_C, C_C\}$$

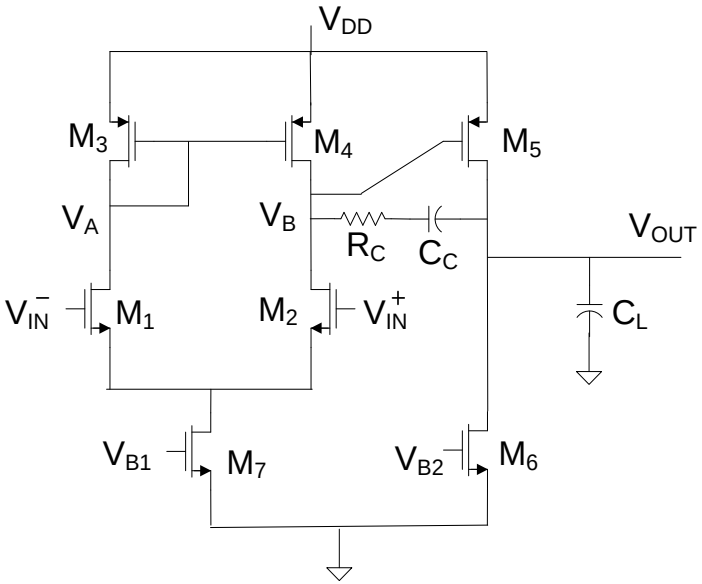
2 constraints (phase margin), $z_1 = p_2 = \dfrac{-g_{m5}}{C_C\left[\dfrac{g_{m5}}{g_C} - 1\right]}$

Design Flow:

1. Ignore R_C and design as if RHP zero is present
2. Pick R_C to cancel p_2
3. Adjust p_1 (i.e. change/reduce C_C) to achieve desired phase margin

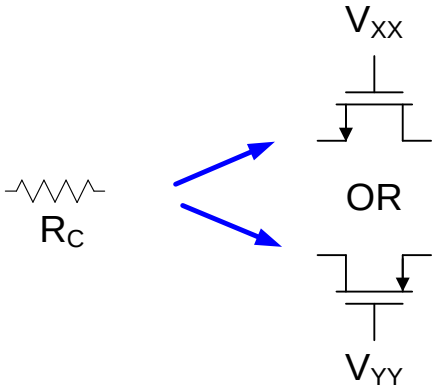
   (or preferably desired closed-loop performance for desired β)

Basic Two-Stage Op Amp with LHP zero



Realization of R_C

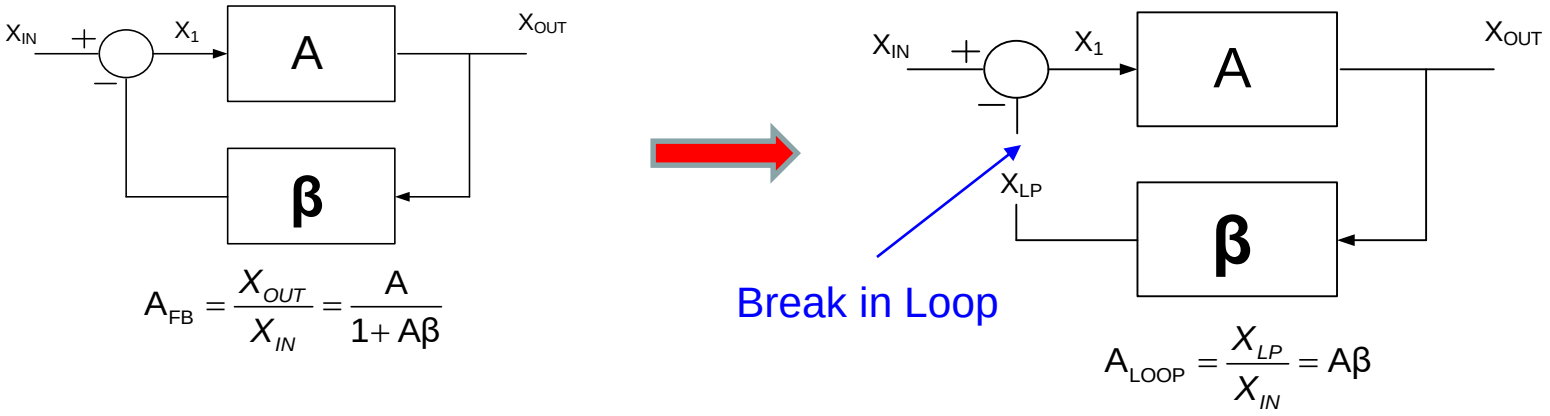
$$R_C = \frac{L}{\mu C_{OX} W V_{EB}}$$



Transistors in triode region
Very little current will flow through transistors (and no dc current)
V_{DD} or GND often used for V_{XX} or V_{YY}
V_{BQ} well-established since it determines I_{Q5}
Using an actual resistor not a good idea (will not track g_{m5} over process and temp)

Two-Stage Amplifiers

Loop Gain Analysis



- Loop Gain
  - Loading of A and β networks
  - Breaking the Loop (with appropriate terminations)
  - Biasing of Loop
  - Simulation of Loop Gain
- Open-loop gain simulations
  - Systematic Offset
  - Embedding in closed loop

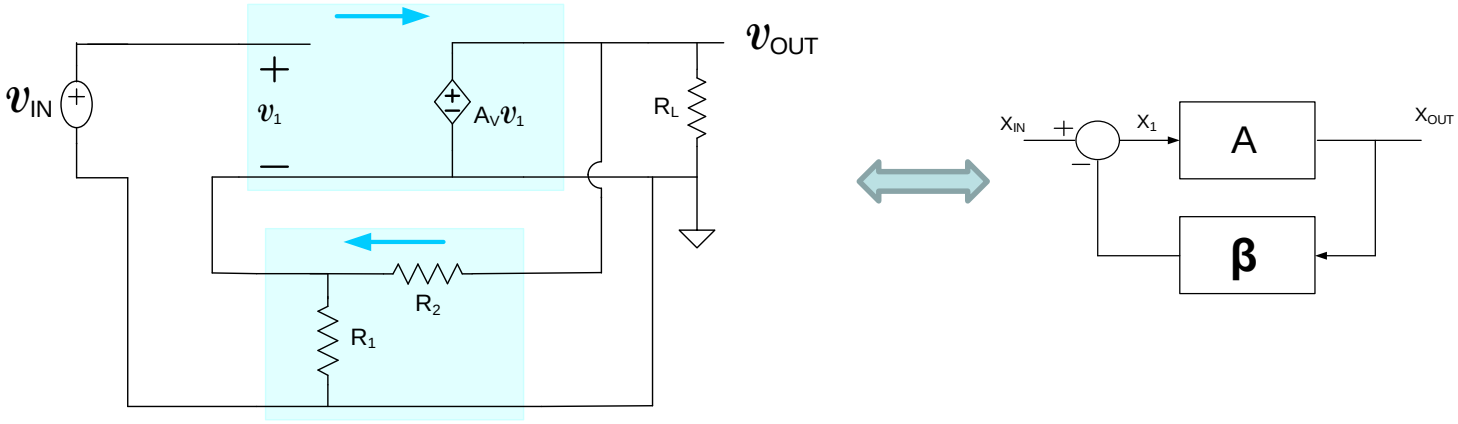
Loop Gain - Aβ

Loop Gain is a Critical Concept for Compensation of Feedback Amplifiers when Using Phase Margin Criteria (If you must!)

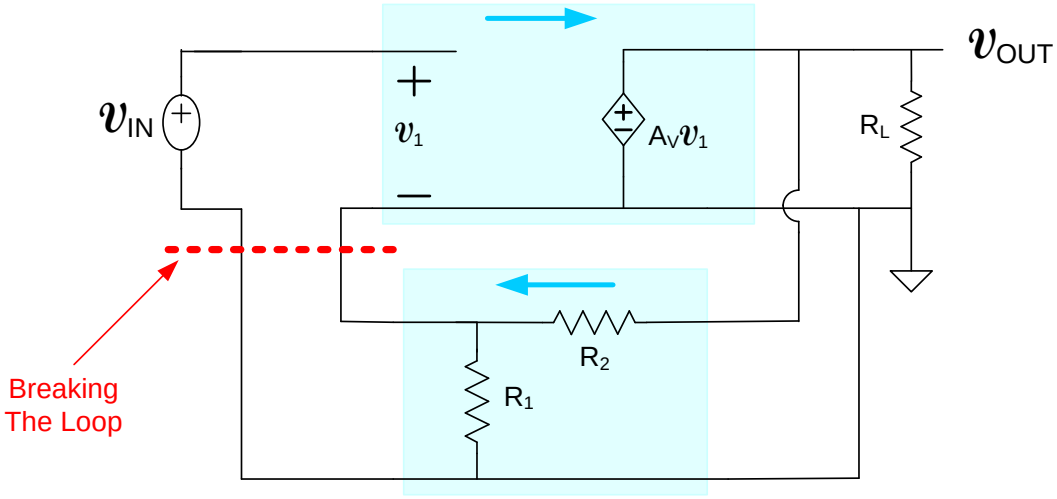
- Sometimes it is not obvious where the actual loop gain is at in a feedback circuit
- The A amplifier often causes some loading of the β amplifier and the β amplifier often causes some loading of the A amplifier
- Often try to “break the loop” to simulate or even calculate the loop gain or the gains A and β
- If the loop is not broken correctly or the correct loading effects on both the A amplifier and β amplifier are not included, errors in calculating loop gain can be substantial and conclusions about compensation can be with significant error

Loop Gain - Aβ

(for voltage-series feedback configuration)

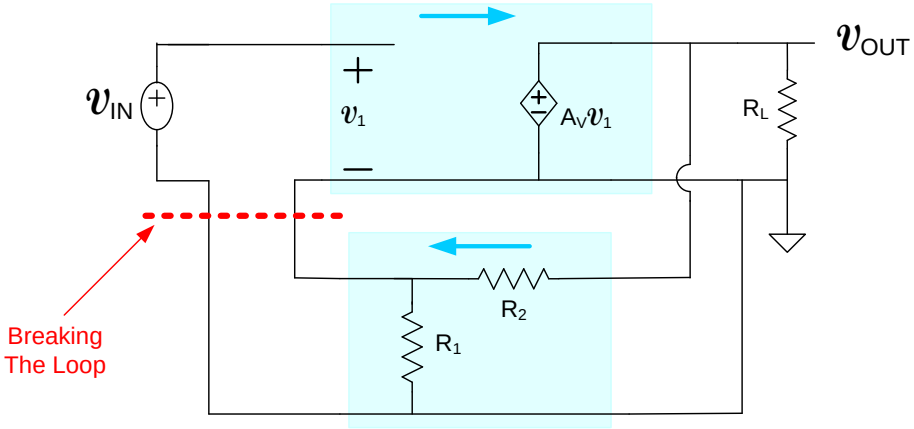


The loop is often broken on the circuit schematic to determine the loop gain



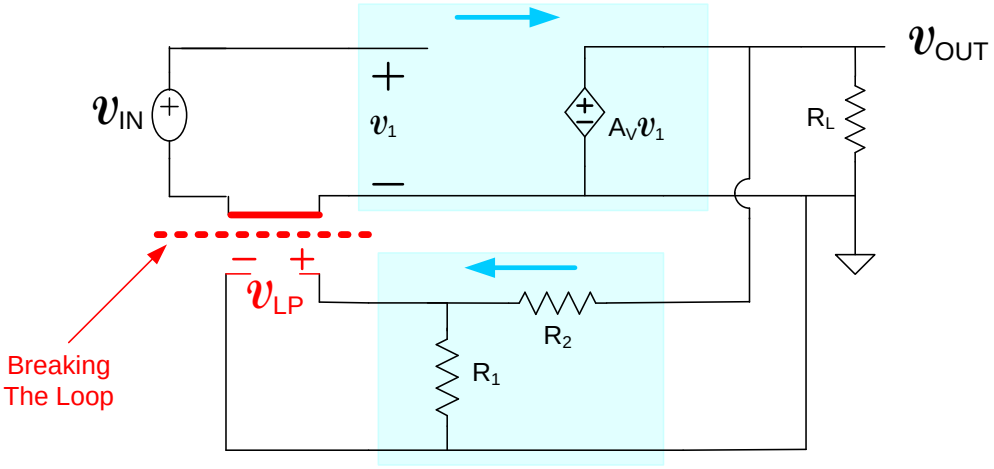
Loop Gain - Aβ

Breaking the loop to obtain the loop gain (Ideal A amplifier)



$$\beta = \frac{R_1}{R_1+R_2}$$

Note terminations where the loop is broken – open and short

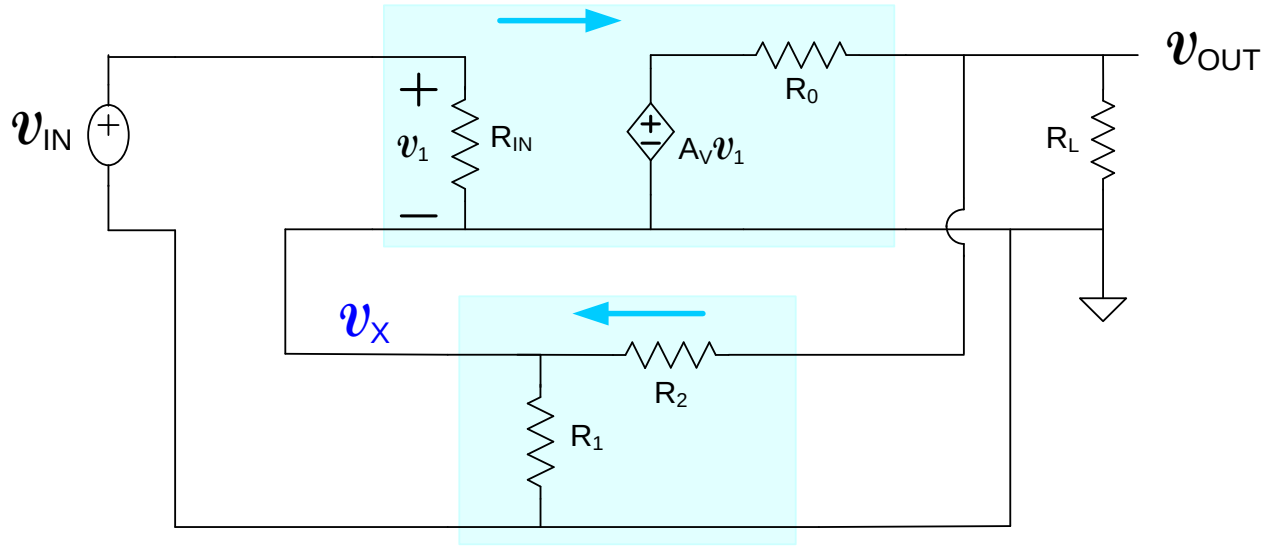


$$v_{LP} = v_{IN} A_V \frac{R_1}{R_1+R_2}$$

$$\frac{v_{LP}}{v_{IN}} = A_{LOOP} = A\beta$$

Loop Gain - Aβ

But what if the amplifier is not ideal?



For the feedback amplifier:

$$\left.\begin{aligned} v_{OUT}\left(G_O+G_L+G_2\right) &= v_X G_2 + A_V v_1\, G_O \\ v_X\left(G_1+G_2+G_{IN}\right) &= v_{OUT} G_2 + v_{IN} G_{IN} \\ v_{IN} &= v_1 + v_X \end{aligned}\right\}$$

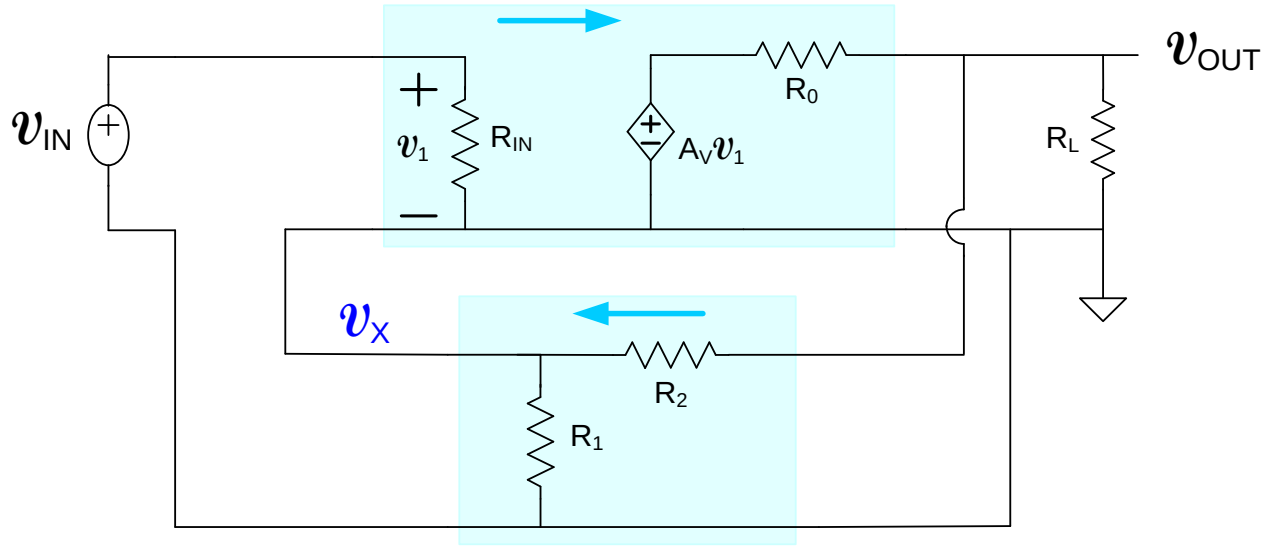
Solving, we obtain

$$A_{FB} = \frac{v_{OUT}}{v_{IN}} = \frac{G_{IN}G_2 + A_V\left(G_O\left[G_1+G_2\right]\right)}{\left(G_O+G_L\right)\left[G_1+G_2+G_{IN}\right] + G_2\left(G_1+G_{IN}\right) + A_V G_2 G_O}$$

What is the Loop Gain ? Needed to obtain the Phase Margin !

Loop Gain - Aβ

But what if the amplifier is not ideal?



$$A_{FB} = \frac{v_{OUT}}{v_{IN}} = \frac{G_{IN}G_2 + A_V\left(G_O\left[G_1+G_2\right]\right)}{\left(G_O+G_L\right)\left[G_1+G_2+G_{IN}\right]+G_2\left(G_1+G_{IN}\right)+A_V G_2 G_O}$$

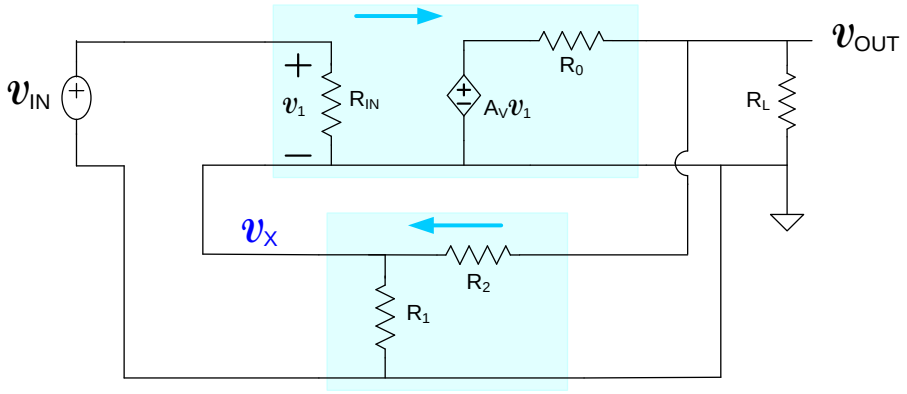
What is the Loop Gain ? Needed to obtain the Phase Margin !

Remember: $A_{FB} = \dfrac{F_1(s)}{1+A\beta}$ Characteristic Polynomial Determined by $D(s) = 1 + A\beta$

Whatever is added to “1” in the denominator is the loop gain

Loop Gain - Aβ

But what if the amplifier is not ideal?



$$\beta = \frac{R_1}{R_1+R_2}$$

$$\beta = \frac{G_2}{G_1+G_2}$$

$$A_{FB} = \frac{v_{OUT}}{v_{IN}} = \frac{G_{IN}G_2+A_V\left(G_O\left[G_1+G_2\right]\right)}{\left(G_O+G_L\right)\left[G_1+G_2+G_{IN}\right]+G_2\left(G_1+G_{IN}\right)+A_V G_2 G_O}$$

Can be rewritten as

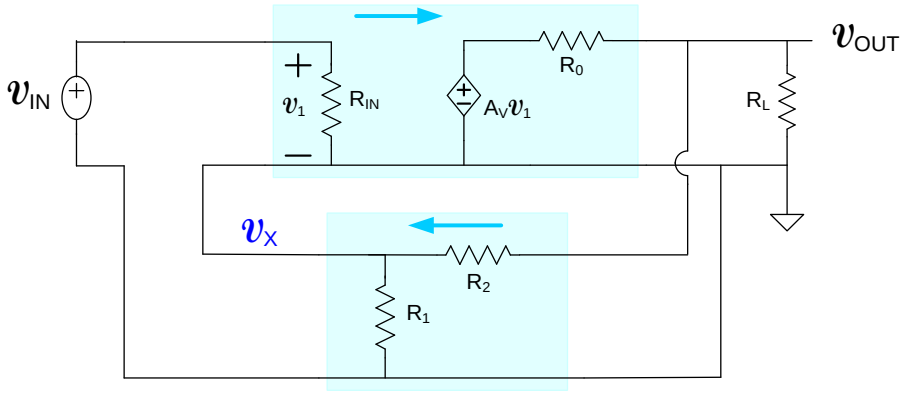
$$A_{FB} = \frac{\dfrac{G_{IN}G_2}{\left(G_O+G_L\right)\left[G_1+G_2+G_{IN}\right]+G_2\left(G_1+G_{IN}\right)}+A_V\left(\dfrac{G_O\left[G_1+G_2\right]}{\left(G_O+G_L\right)\left[G_1+G_2+G_{IN}\right]+G_2\left(G_1+G_{IN}\right)}\right)}{1+A_V\left[\dfrac{G_2G_O}{\left(G_O+G_L\right)\left[G_1+G_2+G_{IN}\right]+G_2\left(G_1+G_{IN}\right)}\right]}$$

The Loop Gain is

$$A_{LOOP} = A_V\left[\frac{G_2G_O}{\left(G_O+G_L\right)\left[G_1+G_2+G_{IN}\right]+G_2\left(G_1+G_{IN}\right)}\right]$$

Loop Gain - Aβ

But what if the amplifier is not ideal?



$$\beta = \frac{R_1}{R_1+R_2}$$

$$\beta = \frac{G_2}{G_1+G_2}$$

The Loop Gain is

$$A_{LOOP} = A_V\left[\frac{G_2 G_O}{(G_O+G_L)[G_1+G_2+G_{IN}]+G_2(G_1+G_{IN})}\right]$$

This can be rewritten as

$$A_{LOOP} = \left(A_V\left[\frac{G_O(G_1+G_2)}{(G_O+G_L)[G_1+G_2+G_{IN}]+G_2(G_1+G_{IN})}\right]\right)\left[\frac{G_2}{G_1+G_2}\right]$$

This is of the form

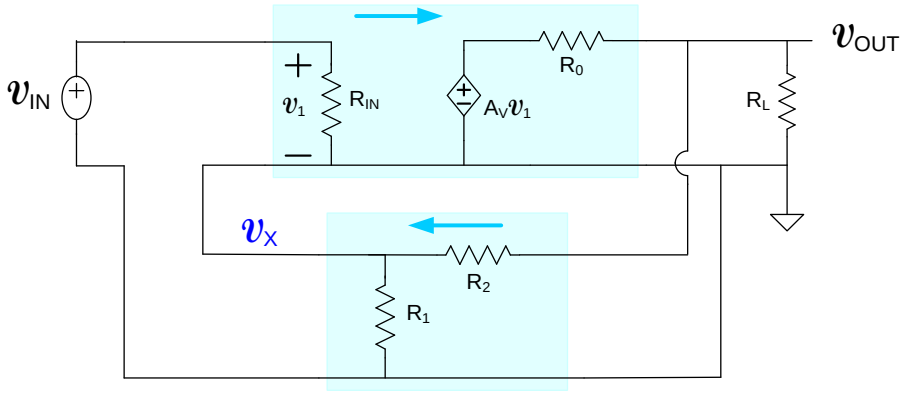
$$A_{LOOP} = (A_{VL})\left[\frac{G_2}{G_1+G_2}\right]$$

where A_{VL} is the open loop gain including loading of the load and β network !

$$A_{VL} = A_V\left[\frac{G_O(G_1+G_2)}{(G_O+G_L)[G_1+G_2+G_{IN}]+G_2(G_1+G_{IN})}\right]$$

Loop Gain - Aβ

But what if the amplifier is not ideal?



$$\beta = \frac{R_1}{R_1+R_2}$$

$$\beta = \frac{G_2}{G_1+G_2}$$

The Loop Gain is

$$A_{LOOP} = A_V\left[\frac{G_2G_O}{(G_O+G_L)[G_1+G_2+G_{IN}]+G_2(G_1+G_{IN})}\right]$$

The Forward Amplifier Gain is

$$A_{VL} = A_V\left[\frac{G_O(G_1+G_2)}{(G_O+G_L)[G_1+G_2+G_{IN}]+G_2(G_1+G_{IN})}\right]$$

Note that A_{VL} is affected by both its own input and output impedance and that of the β network

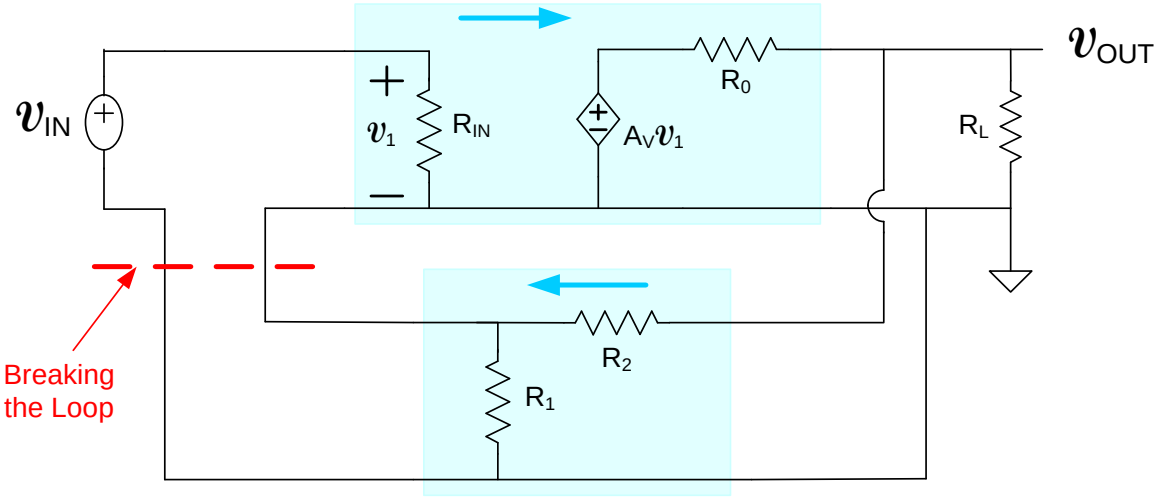
This is a really “messy” expression

Any “breaking” of the loop that does not result in this expression for A_{VL} will result in some errors though they may be small

Loop Gain - Aβ

(for voltage-series feedback configuration)

But what if the amplifier is not ideal?

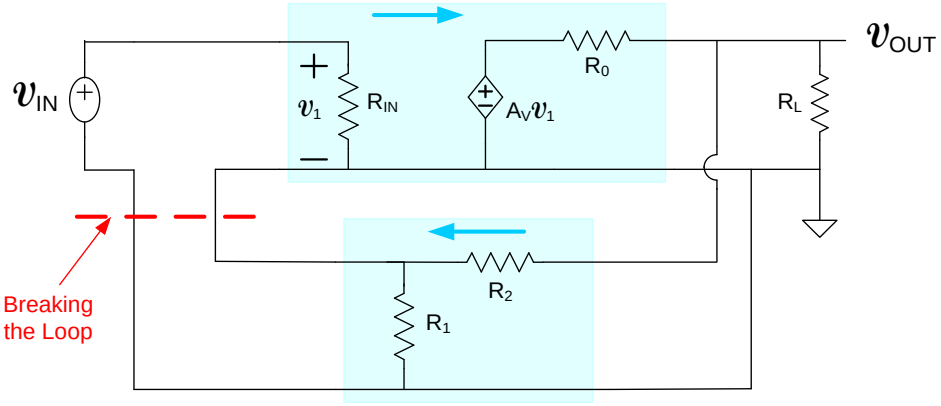


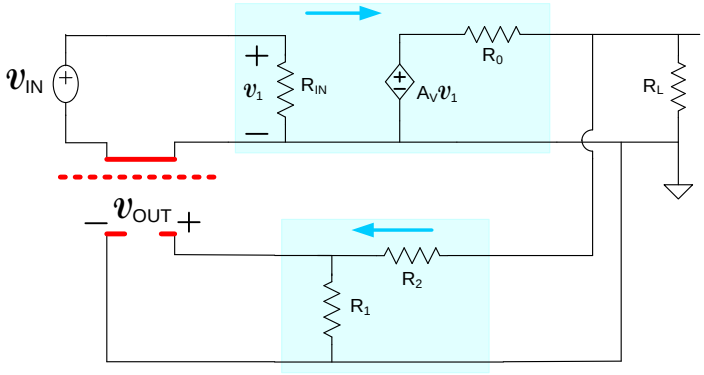
- Most authors talk about breaking the loop to determine the loop gain Aβ
- In many if not most applications, breaking the loop will alter the loading of either the A amplifier or the β amplifier or both
- Should break the loop in such a way that the loading effects of A and β are approximately included
- Consequently, breaking the loop will often alter the actual loop gain a little
- Q-point must not be altered when breaking the loop (for analysis with simulator)
- In most structures, broken loop only gives an approximation to actual loop gain
- Sometimes challenging to break loop in appropriate way

Loop Gain - Aβ

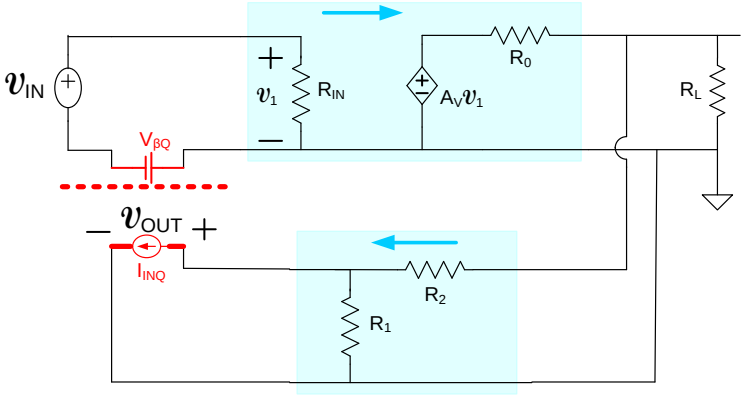
(for voltage-series feedback configuration)

But what if the amplifier is not ideal?





Standard Small-Signal Loop Gain Circuit



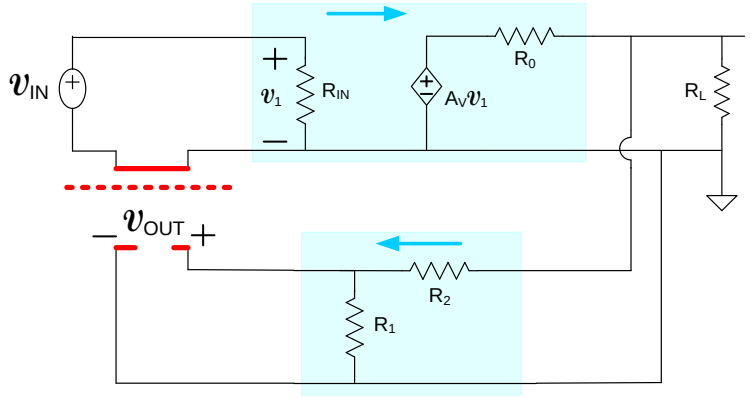
Standard Loop Gain Circuit including Biasing

(terminations shown in ss circuit are what is needed in the actual amplifier)

Loop Gain - Aβ

(for voltage-series feedback configuration)

But what if the amplifier is not ideal?



$$A_{LOOP} = A_V \left[\frac{G_2 G_O}{(G_O + G_L)[G_1 + G_2] + G_2 (G_1)} \right]$$

Loop Gain from Terminated Loop

$$A_{LOOP} = A_V \left[\frac{G_2 G_O}{(G_O + G_L)[G_1 + G_2 + G_{IN}] + G_2 (G_1 + G_{IN})} \right]$$

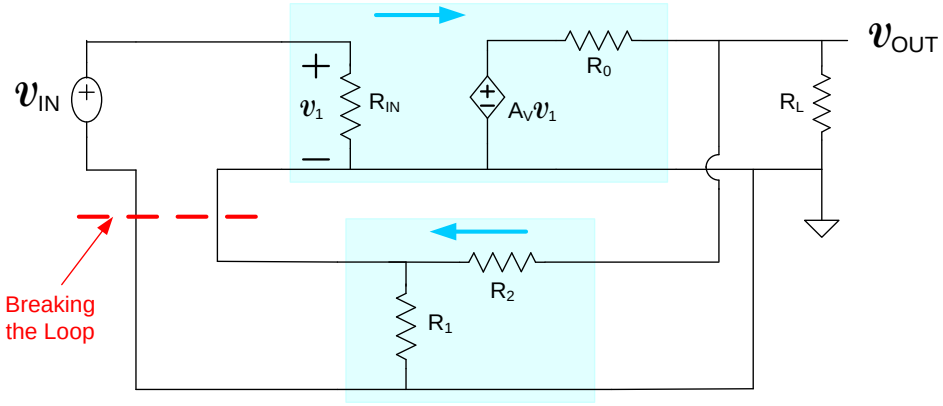
Real Loop Gain

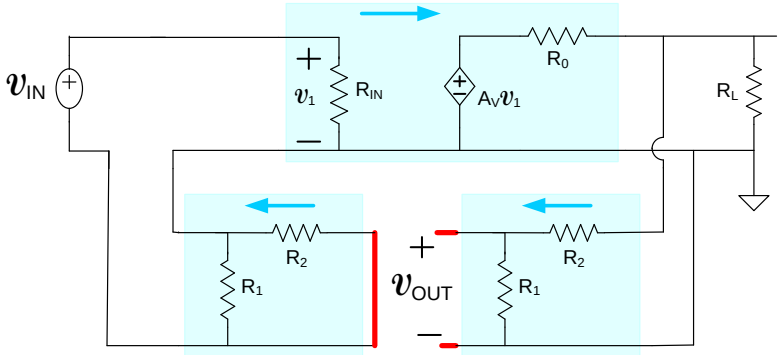
Breaking loop even with this termination will result in some error in A_{LOOP}

Loop Gain - Aβ

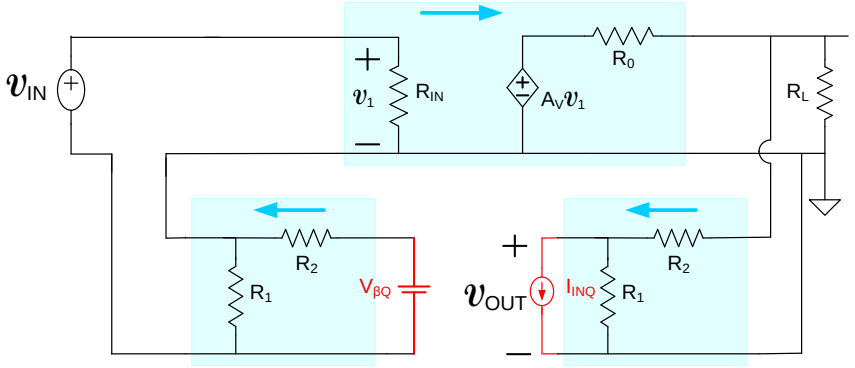
(for voltage-series feedback configuration)

But what if the amplifier is not ideal?





Better Standard Small-Signal Loop Gain Circuit



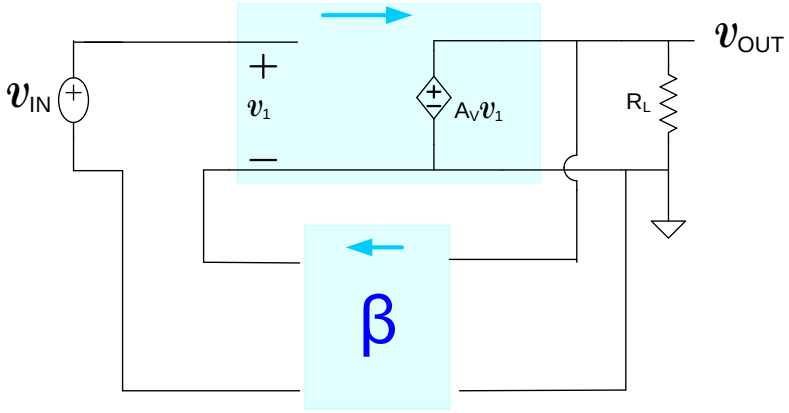
Better Loop Gain Circuit including Biasing

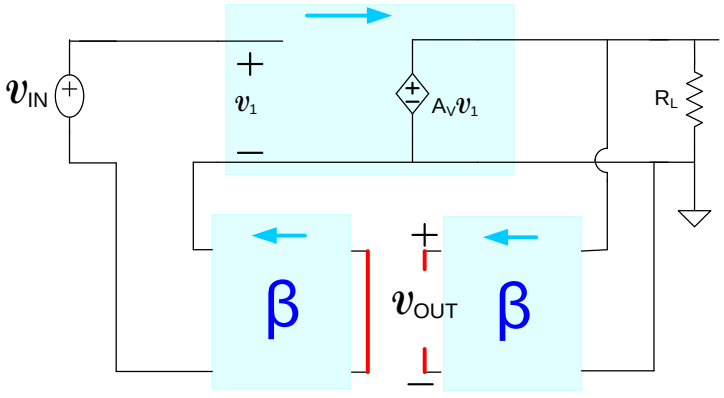
(terminations shown in ss circuit are what is needed in the actual amplifier)

Loop Gain - Aβ

for four basic amplifier types

voltage-series feedback

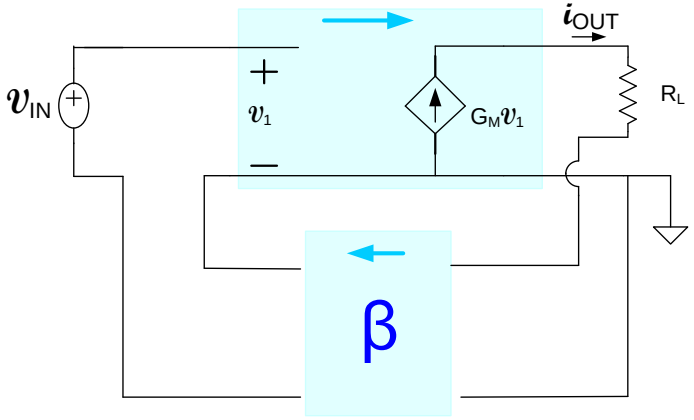


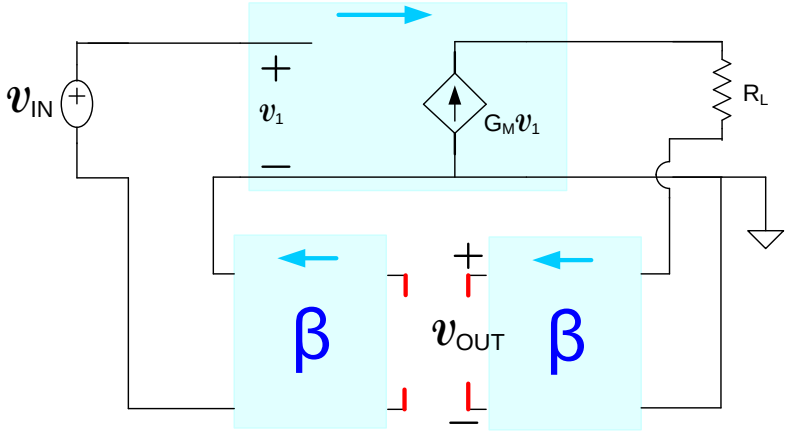


Feedback Amplifier

Loop Gain Amplifier

current-series feedback

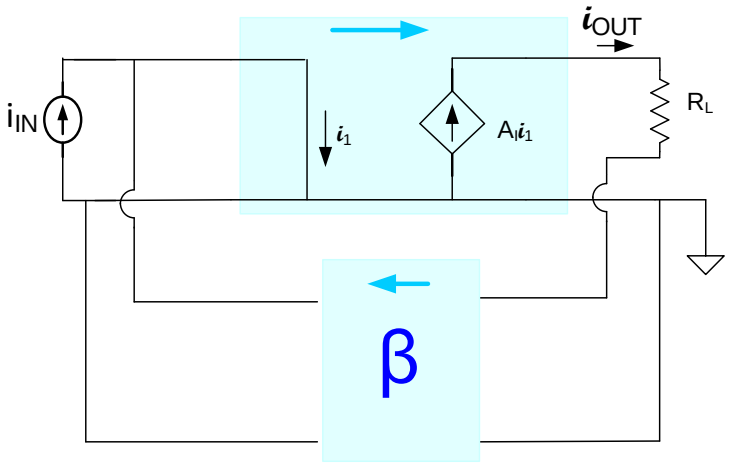


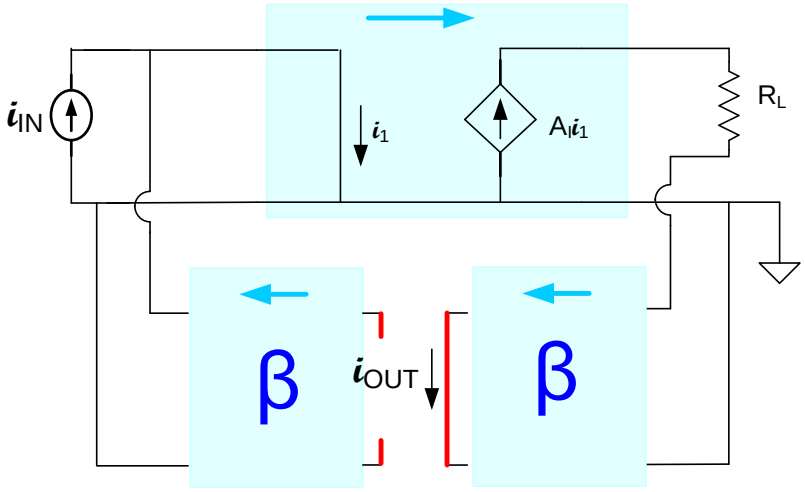


Loop Gain - Aβ

for four basic amplifier types

current-shunt feedback

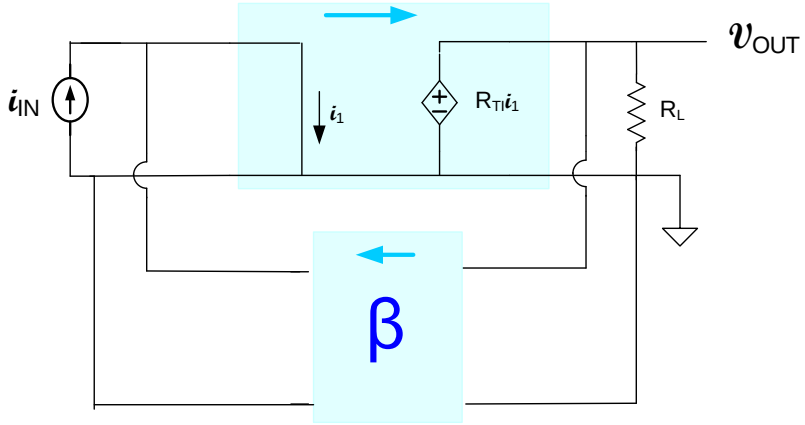


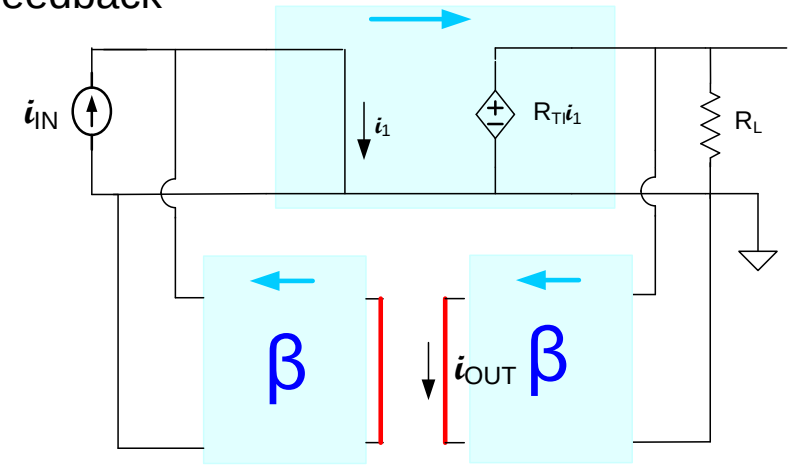


Feedback Amplifier

Loop Gain Amplifier

voltage-shunt feedback





Stay Safe and Stay Healthy !

End of Lecture 18